DEVICE FOR THE CORRECTION OF THE POWER FACTOR IN POWER SUPPLY UNITS WITH FORCED SWITCHING OPERATING IN TRANSITION MODE

CROSS-REFERENCE TO RELATED APPLICATIONS

[1] This application is related to U.S. Patent App. Ser. No. ________ (Atty. Docket No. 2110-75-3) entitled "DEVICE FOR THE CORRECTION OF THE POWER FACTOR IN POWER SUPPLY UNITS WITH FORCED SWITCHING OPERATING IN TRANSITION MODE," which was filed on the same day as the present application and which is incorporated by reference.

PRIORITY CLAIM

[2] This application claims priority from European patent application No. 02425510.1, filed August 1, 2002, and European patent application No. 02425509.3, filed August 1, 2002, which are incorporated herein by reference.

TECHNICAL FIELD

[3] The present invention generally refers to a device for the correction of the power factor in power supply units with forced switching operating in transition mode.

BACKGROUND

[4] These devices are generally used for the active correction of the power factor (PFC) for power supply units with forced switching used in common electronic appliances such as computers, televisions, monitors, etc and to power fluorescent lamps, in other words pre-regulation stages with forced switching which have the task of absorbing from the network supply a current that is virtually sinusoidal and is in phase with network voltage. A power supply unit with forced switching of the present type therefore comprises a PFC and a DC-DC converter connected to the PFC output.

[5] A traditional power supply unit with forced switching comprises a DC-DC converter and an input stage connected to the electric energy distribution network, consisting of a full-wave diode rectifier bridge and of a capacitor connected immediately downstream so as to produce a non-regulated direct voltage from the

network alternating sinusoidal current. The capacitor has sufficiently large capacity because the ripples, *i.e.*, undulation of the voltage across it is relatively small compared with the DC level. The bridge rectifier diodes therefore conduct only a small portion of each half cycle of the network voltage because the momentary value of the network voltage is lower than the voltage on the capacitor for most of the cycle. The current absorbed by the network will accordingly be a series of narrow pulses the amplitude of which is 5 to 10 times the resulting average value.

[6] This has considerable consequences: the current absorbed from the line has peak and effective values that are much greater than in case of the absorption of sinusoidal current, the network voltage is distorted by the almost simultaneous pulsed absorption of all the appliances connected to the network, in the case of three-phase systems the current in the neutral conductor is greatly increased and the energy potential of the system for producing electric energy is poorly used. In fact, the wave shape of a pulsed current is very rich in odd harmonic distortions that, whilst not contributing to the power returned to the load, contribute to increasing the effective current absorbed by the network and therefore to increasing the dissipation of energy.

[7] In quantitative terms this can be expressed in terms of power factor (PF), defined as the ratio between real power (the power that the power supply unit returns to the load plus the power dissipated inside it in the form of heat) and apparent power (the product of the effective network voltage for the effective absorbed current), both in terms of total harmonic distortion (THD), generally defined as the percentage ratio between energy associated with all the harmonic distortions of a superior order and that associated with the fundamental harmonic distortion. Typically, a power supply unit with a capacitive filter has a PF between 0.4-0.6 and a THD greater than 100%.

[8] A PFC arranged between the rectifier bridge and the input of the DC-DC converter enables a virtually sinusoidal current to be absorbed from the network, which current is in phase with the voltage and brings PF close to 1 and reduces THD.

[9] The PFCs generally comprise a converter provided with a power transistor and an inductor coupled to it and a control device coupled to the converter

in such a way as to obtain from a network alternating input voltage a DC voltage regulated at the output. The control device is capable of determining the period of switched-on time Ton and the period of switched-off time Toff of the power transistor; the union of the period of Ton and the period of Toff time gives the cycle period or switching period of the power transistor.

[10] The commercially available PFC circuit types are basically of two kinds that differ according to the different control technique used: pulse width modulation (PWM) control with fixed frequency wherein current is conducted continuously into an inductor of the power supply unit and variable frequency PWM control, also known as 'transition mode' (TM) because the inductor current is reset (*i.e.*, zeroed) exactly at the end of each switching period. TM control can be operated both by controlling inductor current directly or by controlling the period of Ton time. The fixed-frequency control technique provides better performance but uses complex circuit structure whereas TM technique requires a more simple circuit structure. The first technique is generally used with high power levels whilst the second technique is used with medium - low power levels, normally below 200W.

[11] **FIG. 1** is a diagrammatic view of a PFC pre-regulatory stage of the TM type comprising a boost converter ***20*** and a control device ***1***. The boost converter ***20*** comprises a full-wave diode rectifier bridge ***2*** with Vin network voltage input, a capacitor ***C1*** (that is used as a high-frequency filter) with a terminal connected to the diode bridge ***2*** and the other terminal earthed, an inductor ***L*** connected to a terminal of the capacitor ***C1***, an MOS power transistor ***M*** with the drain terminal connected to a terminal of the inductance ***L*** downstream of the latter and having the source terminal connected to a grounded resistance ***Rs***, a diode ***D*** having the anode connected to the common terminal of the inductor ***L*** and the transistor ***M*** and the cathode connected to a capacitor ***Co***, having the other terminal grounded. The boost converter ***20*** generates a DC output voltage Vout on the capacitor ***Co*** that is greater than the network maximum peak voltage, typically 400 V for systems powered by European network supplies or by a universal supply. Said output voltage ***Vout*** will be the input voltage of the DC-DC converter connected to the PFC.

[12] The control device ***1*** has to maintain the output voltage ***Vout*** at a constant value by feedback control. The control device ***1*** comprises an error

amplifier ***3*** suitable for comparing part of the output voltage ***Vout***, in other words the voltage ***Vr*** deriving from Vr=R2*Vout/(R2+R1) (where resistances ***R1*** and ***R2*** are serially connected together and parallel to the capacitor ***Co***) with a reference voltage ***Vref***, for example 2.5V, and generates an error signal proportionate to their difference. The undulation frequency of output voltage ***Vout*** is twice that of the network voltage and is superimposed on the DC value. However, if the bandwidth of the error amplifier is significantly reduced (typically to below 20 Hz) by means of a suitable compensation network comprising at least one capacitor and we assume virtually stationary operation, in other words with constant direct effective input voltage and output load, said undulation will be greatly attenuated and the error signal will become substantially constant.

[13] The error signal ***Se*** is sent to a multiplier ***4***, where it is multiplied by a signal ***Vi*** given by part of the network voltage rectified by the diode bridge ***2***. At the output of the multiplier ***4*** there is a signal ***Sm*** provided as a rectified sinusoidal current, the amplitude of which depends on the effective network voltage and on the error signal.

[14] The signal ***Sm*** is sent to the non-inverting input of a PWM comparator ***5*** whereas the signal ***Srs*** across the resistance ***Rs*** is provided to the inverting input. If the signals ***Srs*** and ***Sm*** are the same, the comparator ***5*** sends a signal to a control block ***6*** that pilots the transistor ***M***, which in this case switches it off. In this way the output signal ***Sm*** of the multiplier determines the peak current of the transistor ***M*** and this is then enveloped by a rectified sinusoidal current. A filter at the stage input eliminates the switching frequency component so that the current absorbed by the network has the form of the sinusoidal envelope.

[15] After the MOS has been switched off the inductor releases the energy stored in it onto the load until it is completely emptied. At this point, the diode opens and the drain node of the MOS continues to float, so that its voltage moves towards the momentary input voltage through resonance oscillations between the stray capacitance of the node and the inductor inductance. The drain voltage is thus rapidly reduced, said drain voltage being coupled to the pin to which a block is connected that detects current ***7*** zeroes, which detector block belongs to the block ***6***, by means of the auxiliary coil of the inductor. The block ***6*** furthermore comprises an

OR gate ***8*** having an input connected to the block ***7*** and the other input connected to a starter ***10***, suitable for sending a signal to the OR gate ***8*** at the instant of initial time; the output signal ***S*** of the OR gate ***8*** is the set input ***S*** of a set-reset flip-flop ***11*** having another input ***R***, which is the output signal of the device ***5***, and having an output signal ***Q***. The Q signal is sent to the input of a driver ***12*** that controls switch-up or switch-off of the M transistor.

[16] A PFC absorbs an almost sinusoidal current that is not completely sinusoidal. There are two main sources of the residual distortion, which tends to maintain a not insignificant THD. The first is undulation with a frequency which is twice that of the network superimposed on the signal ***Se***, if it is at a DC level present leaving the error amplifier, which introduces a 3rd harmonic distortion in the current reference generated by the multiplier. The second is cross distortion, which is seen as a short flat zone in the wave form of the network current ***IR***, corresponding to the network voltage zeroes, which correspond to the minimum values ***VC1min*** of the voltage ***VC1*** across the capacitor ***C1***, as shown in **FIG. 2**, which shows the current ***IR*** and the voltage ***VC1*** across the capacitor C1, in two cases with Vin=220Vac and input Pin power= 80W (**FIG. 2a**) and Vin=220Vac and Pin=40W (**FIG. 2b**). The cross distortion increases as the PFC load decreases and as effective network voltage increases.

[17] The cause of this distortion is the defective transfer of input-output energy that occurs near the zeroes of the network voltage. In this zone the energy stored in the inductor ***L*** is very low, insufficient to load the stray capacitance of the drain node of the MOS to the output voltage ***Vout*** (typically 400V) so as to enable the passage of current through the diode ***D*** and transfer the energy of the inductor ***L*** to output. As a result, the diode is not switched on for a certain number of switching cycles and the energy network remains confined in the resonating circuit consisting of said stray capacitance and of the inductor ***L***. This phenomenon, which is accentuated by the presence of the high frequency filter capacitor ***C1*** after the rectifier bridge, is shown in detail in **FIG. 3**, in which the current ***IR*** and the voltage ***Vdrain*** are shown in a zone in which the current ***IR*** is flat.

SUMMARY OF THE INVENTION

[18] In view of the state of the technique described, an embodiment of the present invention is a device for the correction of the power factor in power supply units with forced switching operating in transition mode that enables cross distortion to be minimised.

[19] According to this embodiment, the device for the correction of the power factor in power supply units with forced switching operating in transition mode, comprises a converter and a control device coupled to said converter so as to obtain from a network alternating input voltage a voltage regulated on the output terminal, said converter comprising a power transistor, said control device comprising a pilot circuit suitable for determining the period of switched-on and switched-off time of said power transistor, characterised in that said control device comprises control means coupled to said pilot circuit and with said converter and which is capable of prolonging said period time during which the transistor is switched at the instants of time in which said network alternating voltage substantially assumes a zero value.

[20] Said converter preferably comprises a rectifier circuit of said network input voltage, said control device comprises an error amplifier that has on the inverting input a first signal that is proportionate to said regulated voltage and on the non-inverting terminal a reference signal and said pilot circuit comprises a multiplier having at the input a second signal that is proportionate to the voltage rectified by said rectifier circuit and an error signal leaving said error amplifier, a comparator suitable for comparing a third output signal from said multiplier and a fourth signal that is proportionate to the current that flows through said power transistor, the fifth output signal from said comparator being suitable for determining the periods of time during which said power transistor is respectively switched on and switched off, said control means being suitable for increasing the value of one of said third or fourth signals at the comparator input at the instants of time in which the network voltage has a value that is substantially zero.

BRIEF DESCRIPTION OF THE DRAWINGS

[21] Characteristics and advantages of the present invention will appear evident from the following detailed description of its embodiments thereof, illustrated as non-limiting examples in the enclosed drawings, in which:

[22] **FIG. 1** is a circuit diagram of a PFC in transition mode for a prior-art power supply unit with forced switching;

[23] **FIGS. 2a**, **2b** show diagrams obtained by an oscilloscope that show the network current and the rectified network voltage taken across the capacitor placed immediately after the rectifier bridge of the PFC of **FIG. 1** with differing input power;

[24] **FIG. 3** shows, around a zero of network voltage, the network current and the voltage on the drain terminal of the MOS terminal of the PFC in **FIG. 1**;

[25] **FIG. 4** is a circuit diagram of a PFC in transition mode for a power supply unit with forced switching according to a first embodiment of the present invention;

[26] **FIG. 5** is a circuit diagram of a PFC in transition mode for a power supply unit with forced switching according to the first embodiment of the present invention;

[27] **FIGS. 6a**, **6b** show diagrams obtained in an oscilloscope that show the network current and the rectified network voltage taken across of the capacitor located immediately after the rectifier bridge of the PFC with **FIG. 5** with differing input power;

[28] **FIG. 7** shows, around a zero of the network voltage, the network current and the voltage on the drain terminal of the MOS transistor of the PFC converter of **FIG. 5**;

[29] **FIGS. 8a-8b** show the percentage value of the THD for the PFC of **FIG. 1** and for the PFC of **FIG. 5** with differing output power;

[30] **FIG. 9** is a block diagram of a PFC circuit in transition mode for a power supply unit with forced switching according to a second embodiment of the present invention;

[31] **FIG. 10** shows the wave forms of significant signals of the circuit in **FIG. 9**;

[32] **FIGS. 11a-11b** show circuit diagrams of the multiplier in **FIG. 1** and of the circuit in **FIG. 9**;

[33] **FIGS. 12a**, **12b** show diagrams obtained in an oscilloscope that show the network current and the rectified network voltage taken across the capacity located immediately after the rectifier bridge of the PFC according to the second embodiment of the present invention with differing input power;

[34] **FIG. 13** shows, around a zero of the network voltage, the network current and the voltage on the drain terminal of the MOS transistor of the PFC converter according to the second embodiment of the present invention;

[35] **FIG. 14** is a diagram of another circuit of a PFC in transition mode for a power supply unit with forced switching according to a variation of the second embodiment of the present invention.

DETAILED DESCRIPTION

[36] **FIG. 4** shows a PFC for a power supply unit with forced switching operating in transition mode according to a first embodiment of the invention; the elements that are the same as the circuit in **FIG. 1** will be indicated by the same references. The PFC comprises a boost converter ***20*** provided with a full-wave diode rectifier bridge **2** that has a network input voltage ***Vin***, a capacitor ***C1*** that has a terminal connected to the diode bridge ***2*** and the other terminal grounded, an inductor L connected to a terminal of the capacitor ***C1***, a MOS ***M*** power transistor with its drain terminal connected to a terminal of the inductor ***L*** downstream of the latter and having the source terminal connected to a grounded resistance ***Rs***, a diode ***D*** with its anode connected to the terminal shared by the inductor ***L*** and the transistor ***M*** and the cathode connected to a capacitor ***Co***, the other terminal of which is grounded. The boost converter ***20*** generates a DC output voltage ***Vout*** that is greater than the network maximum peak voltage, typically 400 V for systems powered by European network or by universal power supplies.

[37] The PFC comprises a control circuit ***100*** suitable for maintaining the output voltage ***Vout*** at a constant value by means of feedback control. The control

circuit ***100*** comprises an error amplifier ***3*** suitable for comparing part of the output voltage ***Vout***, in other words the voltage ***Vr*** supplied by Vr=R2*Vout/(R2+R1) (where resistances R1 and R2 are serially connected together and are connected parallel to the capacitor ***Co***) with a reference voltage ***Vref***, for example 2.5V, and generates an error signal proportionate to their difference. Output voltage Vout presents an undulation, the frequency of which is twice that of the network supply and is superimposed on the DC value. If, however, the bandwidth of the error amplifier band is significantly reduced (typically below 20 Hz) by means of a suitable compensation network comprising a capacitor and we assume that operation is almost stationary, in other words with constant effective input voltage and constant output load, said undulation will be greatly attenuated and the steady-status error signal is substantially constant.

[38] The error signal ***Se*** is sent to the input of a control block ***51*** that also has an input signal ***Vi*** that is proportionate to the network voltage ***Vin*** rectified by the diode bridge ***2***, a signal ***S*** that indicates the state of magnetization of the inductor ***L*** and a signal ***Srs*** that is proportionate to the current that flows through the transistor ***M***. Referring to **FIG. 1**,The block ***51*** comprises the multiplier ***4***, the PWM comparator ***5*** and the control block ***6*** and is suitable for determining the period of switched-on time ***Ton*** and the period of switched-off time ***Toff*** of the MOS transistor ***M***.

[39] A circuit block ***50*** according to the first embodiment of the invention has signals ***Vi*** and/or ***Se*** and sends a signal ***Contr*** that enables the switched-on period ***Ton*** of the transistor ***M*** to be prolonged near the zeroes of the network voltage ***Vin***, in other words when the network voltage assumes the value of a few Volts (for example ***2V***), a value that can be considered to be zero compared with the peak value of the network voltage.

[40] **FIG. 5** shows a PFC for a power supply unit with forced switching operating in transition mode according to the first embodiment of the present invention; the elements which are the same as the circuits of **FIGS. 1** and **4** will be indicated with the same references. In **FIG. 5** the block ***51*** has been explained and comprises the multiplier ***4*** with input signals ***Vi*** and ***Se*** that sends a signal ***Sm*** to the non-inverting input of a PWM comparator ***5*** the output signal of which is on the input

of the block ***6***. In the inverting input of the comparator ***5*** the signal ***Contr*** on the output of block ***50*** is present.

[41] The latter comprises a resistance ***Ra*** connected on the one hand to the source terminal of the transistor ***M*** and to a terminal of the resistance ***Rs*** and on the other to the inverting input of the comparator ***5*** so as to take the signal ***Srs*** to the inverting input of the comparator. The block ***50*** also comprises a resistance ***Rb*** connected to the inverting input of the comparator ***5*** and to the anode of a diode ***Di*** and with a capacitor ***Ci***, the other terminal of which is grounded. The cathode of the diode ***Di*** is connected to the auxiliary coil ***L1*** of the inductor ***L***.

[42] During the period of switched-on time ***Ton*** of the MOS transistor ***M***, when the voltage across the auxiliary coil ***L1*** is negative, the diode ***Di*** enables charging of the capacitor ***Ci***. In this way the negative voltage on the node ***P*** is proportionate to effective network voltage and depends on the turn ratio of the auxiliary coil ***L1***. The resistance ***Rb*** provides this negative voltage, in other words an offset of negative voltage, in addition on the inverting node of the comparator ***5*** at the signal ***Srs***.

[43] A resistance ***Rc*** can be inserted between the output of the error amplifier ***3*** and the inverting input of the comparator ***5***; in this way there is a variation in the offset of negative voltage as the output load varies because the voltage signal ***Se*** has a value that lowers as the input voltage ***Vin*** increases and the load decreases.

[44] This solution produces a negative voltage offset during a semi-period of the network voltage ***Vin***, nevertheless, the value of said voltage ***Vin*** in instants of time that are different from the instants in which said voltage is near zero is very high and the voltage offset does not have a substantial effect.

[45] To preferably modulate said offset with the instant value of the network voltage so that the latter is less negative when it is far from the time instants in which the network voltage ***Vin*** assumes a zero value, a positive voltage component can be added to said offset that is zero near said zeroes of the network voltage ***Vin***. This can be done by picking up the signal ***Vi*** at the input of multiplier ***4*** by means of the resistance ***Rd*** and taking it to the inverting input of the comparator ***5***.

[46] The negative voltage offset influences the output signal from the comparator ***5*** in such a way as to determine a prolongation of the period of switched-on time ***Ton*** of the MOS transistor ***M***.

[47] To calibrate the circuit, one of the two resistances ***Ra*** and ***Rb*** can be fixed and the other one can be varied; calibrating is typically carried out with network voltage ***Vin*** at its maximum value, in other words in the conditions in which, generally, THD is at maximum in order to determine the overall resistance value that has the lowest THD.

[48] The effects of the correction made by the circuit ***50*** of **FIG. 5** are shown in **FIGS. 6a, 6b** and **7**.

[49] **FIGS. 6a, 6b** show diagrams obtained in an oscilloscope that show the network current ***IR*** and the voltage ***VC1*** across the capacitor ***C1*** with a respective voltage of Vin=220VAC and pin power = 80W, and with Vin voltage =220VAC and Pin power =40W.

[50] **FIG. 7** shows, around a zero of the network voltage, the network current ***IR*** and the voltage ***Vdrain*** on the drain terminal of the MOS transistor ***M***.

[51] **FIGS. 8a** and **8b** show the values of total harmonic distortion THD1 and THD2 respectively for the circuit of **FIG. 5** and for the circuit of **FIG. 1** with output power Pout=80W (**FIG. 8a**) and with output power Pout=40W (**FIG. 8b**).

[52] **FIG. 9** shows a block diagram of a circuit of a PFC for a power supply unit with forced switching operating in transition mode according to a second embodiment of the present invention. Said circuit comprises the block ***50*** of **FIG. 4** and the multiplier ***4*** that has the input signals ***Vi*** and ***Se*** the provides the output signal ***Sm***; the signal ***Contr*** leaving block ***50*** is sent to the non-inverting input of the comparator ***5***.

[53] The block ***50*** enables a positive voltage offset to be added to the signal ***Sm*** leaving the multiplier ***4*** only during the instants of time in which the network voltage ***Vin*** has a value close to zero. The positive voltage offset is higher the higher is the network voltage ***Vin*** and the lower is the output load. The positive voltage offset is created by adding to the signal ***Sm*** from the multiplier ***4*** a small portion of the signal present on one of its inputs, in other words a portion of the signal ***Vi*** or a

portion of the signal ***Se*** so as to obtain the signal ***Contr*** that is sent to the non-inverting input of the comparator ***5***. The positive voltage offset can also be achieved by adding portions of both the signals ***Se*** and ***Vi*** to the signal ***Sm*** to obtain the signal ***Contr***.

[54] The signal ***Vi*** is subtracted from a signal ***A2***, which has a value that remains constant over time and the resulting signal is multiplied by a constant ***K2*** in order to obtain the signal ***Vi1*** that is added to the signal ***Sm*** to obtain the signal ***Contr***.

[55] Alternatively, or additionally, the signal ***Se*** is subtracted from a signal ***A1***, which has a value that remains constant over time and the resulting signal is multiplied by a constant ***K1*** in order to obtain the signal ***Se1*** that is added to the ***Sm*** signal to obtain the signal ***Contr***.

[56] **FIG. 10** shows the time wave forms of the signals ***Se***, ***Vi***, ***Sm*** and ***Contr*** of **FIG. 9**; the latter differs from the signal ***Sm*** above by the fact that it does not take on the value zero.

[57] **FIGS. 11a-11b** show diagrams of a possible circuit embodiment of the multiplier ***4*** of **FIG. 1** and of the circuit of **FIG. 9** comprising the multiplier ***4*** and the block ***50***. The multiplier of **FIG. 11a** comprises an input stage provided with differential first and second stage. The first differential stage comprises two bipolar pnp transistors with collector terminals coupled to a voltage supply VDD and connected to a current generator ***I1*** and grounded emitter terminals, and the second differential stage comprises two bipolar pnp transistors with collector terminals coupled to a voltage supply VDD and connected to a current generator ***I2*** and the grounded emitter terminals. The base terminal of one of the transistors of the first stage is connected to the voltage ***Vi*** whilst the base terminal of the other transistor isgrounded, the base terminal of one of the transistors of the second stage is connected to the voltage ***Se*** whilst the base terminal of the other transistor is connected to a 2.5 V reference voltage supply ***V2***. The outlets of the two differential stages are at the input of an intermediate stage that pilots a current generator ***Io*** of an output stage that in turn flows along a resistance ***R***. The signal ***Sm*** is given by Sm=Io*R.

[58] The circuit in **FIG. 11b** is a circuit embodiment of the block ***50*** and of the multiplier ***4*** of **FIG. 9**. Said circuit differs from the one in **FIG. 11a** because instead of the resistance ***R*** there are three resistances ***R10***, ***R20*** and ***R30*** connected serially to one another and because the terminals of the emitter of the transistors of the first and second differential stages having their gate terminals connected respectively to signals ***Vi*** and ***Sm*** are connected respectively to the terminals of the resistances ***R10*** and ***R20*** and to the terminals of the resistances ***R20*** and ***R30***. The outputs of the two differential stages are always at the input of an intermediate stage that pilots a current generator ***Iov*** of an output stage, which output stage in turn flows along the series of resistances ***R10***, ***R20*** and ***R30***. The signal ***Contr*** is given by:

Contr=Iov*(R10+R20+R30)+I1a*(R20+R30)+I2a*R30

where I1a and I2a are the currents that circulate respectively in the first and second stage differential transistors with gate terminals connected respectively to the signals ***Vi*** and ***Sm***.

[59] **FIGS. 12a, 12b** show diagrams obtained from an oscilloscope reading of an embodiment of the circuits in **FIGS. 4** and **5**, the diagrams showing the network current ***IR*** and the voltage ***VC1*** across the capacity ***C1*** with respectively a voltage Vin = 220VAC and pin power = 80W, and with voltage Vin = 220VAC and pin power=40W.

[60] **FIG. 13** shows, around a zero of the network voltage, the network current ***IR*** and the voltage ***Vdrain*** on the drain terminal of the MOS transistor ***M*** for one embodiment of the circuits of **FIGS. 4** and **5**.

[61] **FIG. 14** shows a circuit diagram of a PFC in transition mode for a power supply unit with forced switching according to a variation of the second embodiment of the present invention. Said circuit comprises the block ***50*** of **FIG. 4** and the multiplier ***4*** that has the signals ***Vi*** and ***Se*** at the input and provides the output signal ***Sm***; the signal ***Contr*** at the block ***50*** output is sent to the non-inverting input of the comparator ***5***.

[62] The block ***50*** enables a positive voltage offset to be added to the signal ***Sm*** at the multiplier ***4*** output only during the instants of time wherein the network voltage ***Vin*** has a value near zero. The positive voltage offset is higher the higher is

the network voltage ***Vin*** and lower the lower is the output voltage. The positive voltage offset is created by adding a portion of the signal ***Se*** to the signal ***Sm*** in order to form the signal ***Contr*** to send to the non-inverting input of the comparator ***5***. Nevertheless, this addition is made only when the signal ***Vi*** is lower than a reference value Vth, which is preferably given by the signal ***Se2*** for a constant ***K3***; a comparator ***52*** in fact compares the signals ***Vi***, which persists on the inverting input, and Vth, which persists on the non-inverting input, and if Vi<Vth sends a signal to a switch ***SW*** that enables the addition of the signal ***Se2*** to the signal ***Sm***.

[63] The signal **Se** is subtracted from a signal ***A4*** of a value that remains constant over time and the resulting signal is multiplied by a constant ***K4*** so as to obtain the signal ***Se2*** that is added to the signal ***Sm*** to obtain the signal ***Contr***.

[64] The circuits of **FIGS. 9** and **14** can be integrated into the same chip with the block ***51*** and the error amplifier ***3*** of the control circuit ***100***.

[65] Furthermore, the circuits of **FIGS. 4** and **5** can be incorporated into an electronic system such as a computer system.

[66] From the foregoing it will be appreciated that, although specific embodiments of the invention have been described herein for purposes of illustration, various modifications may be made without deviating from the spirit and scope of the invention.